NON-ABRUPT SWITCHING OF SLEEP TRANSISTOR OF POWER GATE STRUCTURE

ABSTRACT

A semiconductor integrated circuit including a non-abrupt switching mechanism for a sleep transistor of a power gate structure to reduce ground bounce is provided. The semiconductor integrated circuit comprises a supply voltage line; a ground voltage line; a virtual ground voltage line; a logic circuit coupled to the supply voltage line and the virtual ground voltage line; at least one sleep transistor for controlling current flow to the logic circuit, the sleep transistor being coupled to the virtual ground voltage line and the ground voltage line; and a non-abrupt switching circuit for sequentially controlling the sleep transistor. The switching mechanism reduces the magnitude of voltage glitches on the power and ground rails as well as the minimum time required to stabilize power and ground.